Amendments to the Claims:

1. (Currently amended) A junction varactor comprising:

a gate finger lying across an ion well of a semiconductor substrate;

a gate dielectric situated between said gate finger and said ion well;

a first ion diffusion region with first conductivity type located in said ion well at one side of said gate finger;

a first lightly doped drain (LDD) having said first conductivity type in said ion well, and wherein said first LDD merges with said first ion diffusion region serving as an anode of said junction varactor and said first LDD extends laterally to said gate finger; and

a second ion diffusion region with a second conductivity type opposite to said first conductivity type, said second ion diffusion region being located in said ion well at the other side of said gate finger, said second ion diffusion region serving as a cathode of said junction varactor[[.]] ; and

a second lightly doped drain (LDD) of said second conductivity type opposite to said first conductivity type in said ion well, and wherein said second LDD merges with said second ion diffusion region and extends laterally to said gate finger.

2. (Original) The junction varactor according to claim 1 wherein the ion well has said second conductivity type.

3. (Original) The junction varactor according to claim 1 wherein said ion well is electrically isolated by shallow trench isolation (STI).

4. (Canceled)

5. (Canceled)

6. (Currently amended) The junction varactor according to claim 1 wherein said junction varactor further comprises a spacer located on sidewalls of said gate finger.

7. (Currently amended) The junction varactor according to claim 1 wherein said junction varactor further comprises a salicide layer formed on said gate finger and on said first and second ion diffusion regions.

8. (Original) The junction varactor according to claim 1 wherein, in operation, said gate of said junction varactor is biased to a gate voltage V_G that is not equal to 0 volt.

9. (Previously presented) The junction varactor according to claim 1 wherein said gate finger is a metal gate.

10. (Previously presented) The junction varactor according to claim 1 wherein said gate finger is a polysilicon gate.

11. (Original) The junction varactor according to claim 1 wherein said first conductivity type is N type and said second conductivity type is P type.

12. (Currently amended) A junction varactor comprising:

an N well formed in a semiconductor substrate;

a first gate finger lying across said N well;

a first gate dielectric interposed between said first gate finger and said N well;

a second gate finger lying across said N well at one side of said first gate finger;

a second gate dielectric interposed between said second gate finger and said N well;

a P^+ ion diffusion region located in said N well between said first and second gate fingers;

a P type lightly doped drain (PLDD) merging with said P^+ ion diffusion region serving as an anode of said junction varactor and said PLDD extending to said first gate finger and said second gate finger;

a first N^+ ion diffusion region located in said N well at one side of said first gate that is opposite to said P^+ ion diffusion region; [[and]]

a first N type lightly doped drain (NLDD) merging with said first N^+ ion diffusion region and extends laterally to said first gate finger;

a second N^+ ion diffusion region located in said N well at one side of said second gate that is opposite to said P^+ ion diffusion region, wherein said first N^+ ion diffusion region and said second N^+ ion diffusion region are electrically coupled together and serve as a cathode of said junction varactor[[.]] ; and

a second NLDD merging with said second N^+ ion diffusion region and extends laterally to said second gate finger.

13. (Original) The junction varactor according to claim 12 wherein, in operation, said first and second gate fingers of said junction varactor are biased to a gate voltage V_G that is not equal to 0 volt.

14. (Original) The junction varactor according to claim 13 wherein said gate voltage V_G is V_{CC}.

15. (Withdrawn) A junction varactor comprising:

a P well formed in a semiconductor substrate;

a first gate finger lying across said P well;

a first gate dielectric interposed between said first gate finger and said P well

a second gate finger lying across said P well at one said of said first gate finger;

a second gate dielectric between said second gate finger and said P well;

an N^+ ion diffusion region located in said P well between said first and second gate

fingers, said N^+ ion diffusion region serving as an anode of said junction varactor;

a first P^+ ion diffusion region located in said P well at one said of said first gate that is opposite to said N^+ ion diffusion region; and

a second P^+ ion diffusion region located in said P well at one said of said second gate that is opposite to said N^+ ion diffusion region, wherein said first P^+ ion diffusion region and said second P^+ ion diffusion region are electrically coupled together and serve as a cathode of said junction varactor.

16. (Withdrawn) The junction varactor according to claim 15 wherein, in operation, said first and second gate fingers of said junction varactor are biased to a gate voltage V_G that is not equal to 0 volt.

17. (Withdrawn) The junction varactor according to claim 16 wherein said gate voltage V_G is V_{SS}.